

WHAT IS CLAIMED IS:

- 1 1. An access cell for an integrated circuit having a current
2 pathway disposed therein for routing current through said access cell, said
3 current pathway comprising:
4 a first current path disposed lengthwise in said access cell;
5 a second current path disposed lengthwise in said access cell; and
6 a third current path disposed between said first current path and
7 said second current path, said third current path having a set of three legs;
8 a first of said legs being disposed generally parallel to said first
9 and said second current paths;
10 a second of said legs connecting said first current path to said first
11 leg; and,
12 a third of said legs connecting said first leg to said second current
13 path.
- 1 2. The access cell of claim 1 wherein said first, second and
2 third legs are parallel to each other.
- 1 3. The access cell of claim 1 wherein said second and third
2 legs are generally perpendicular to said first, second and third current paths.
- 1 4. The access cell of claim 1 wherein said first, second and
2 third current paths extend substantially the length of the cell.

1 5. The access cell of claim 1 further comprising:
2 a cut point disposed on said first leg, said cut point designating a
3 region of said first leg at which said first leg may be physically severed; and,
4 at least one connect point disposed on said first leg, said at least
5 one connect point designating a region of said first leg at which said first leg
6 may be connected to a net.

1 6. The access cell of claim 2 wherein said cut point is
2 separated from said connect point by at least a minimum allowable distance,
3 wherein said minimum allowable distance is specified in a set of spacing rules
4 associated with said integrated circuit.

1 7. The access cell of claim 1 wherein the first current path is
2 separated from said third current path by at least a minimum allowable
3 distance, wherein said minimum allowable distance is specified in a set of
4 spacing rules associated with said integrated circuit.

1 8. The access cell of claim 1 wherein said first current path is
2 disconnected from said second current path by severing said first leg of said
3 third current path.

1 9. The access cell of claim 8 wherein said first leg of said
2 third current path comprises a first end at which said first leg is connected to
3 said third leg, and a second end at which said first leg is connected to said
4 second leg and wherein said first leg is severed between said first and second
5 ends to cause first current path to be disconnected from said second current
6 path.

1 10. The access cell of claim 1 wherein said first current path is
2 adapted and configured to be connected to a first net, said first net being
3 connectable to said first current path at any location on the first current path,
4 and further wherein said second current path is adapted and configured to be
5 connected to a second net, said second net being connectable to said second
6 current path at any location on the second current path.

1 11. The access cell of claim 10 wherein said first leg of said
2 third current path is severable.

1 12. The access cell of claim 1 wherein said first leg is adapted
2 and configured to connect to a net, said net being connectable to said first leg at
3 a connect point, said connect point designating a region of said first leg at
4 which said first leg is connectable to any net.

1 13. The access cell of claim 1 wherein said current pathway
2 comprises a wire disposed in a metal layer associated with said integrated
3 circuit.

1 14. A method for reconfiguring a current pathway disposed in
2 an access cell, wherein said current pathway comprises a first current path
3 coupled to a second current path via a third current path, said first, second and
4 third current paths being disposed lengthwise in said access cell, wherein said
5 third current path includes a first leg disposed between said first and said
6 second current paths, a second leg connecting said first current path to said first
7 leg, and a third leg connecting said second current path to said first leg, and
8 further wherein said current pathway enables current flow between a first net
9 coupled to said first current pathway and a second net coupled to said second
10 current pathway, said method comprising the steps of:

11 severing said first leg of said third current path to interrupt said
12 current flow from said first net to said second net; and,

13 connecting a third net to said first leg of said third current path at
14 a location on said first leg that allows current to flow between said third net and
15 said second net.

1 15. A method for reconfiguring a current pathway disposed in
2 an access cell, wherein said current pathway comprises a first current path
3 coupled to a second current path via a third current path, said first, second and
4 third current paths being disposed lengthwise in said access cell, wherein said
5 third current path includes a first leg disposed between said first and said
6 second current paths, a second leg connecting said first current path to said first
7 leg, and a third leg connecting said first leg to said second current path, and
8 further wherein said current pathway enables current flow between a first net
9 coupled to said first current pathway and a second net coupled to said second
10 current pathway, said method comprising the steps of:
11 severing said first leg of said third current path to interrupt said
12 current flow from said first net to said second net; and,
13 connecting a third net to said first leg of said third current path at
14 a location on said third net that allows current to flow between said third net
15 and said first net.

1 16. A method for enabling the automatic insertion of an access
2 cell into an integrated circuit design, said method comprising the steps of:
3 modifying a standard definition of said access cell stored in a cell
4 library;
5 identifying a net to which said access cell shall be coupled;
6 modifying a netlist so that said net is represented in said netlist as
7 two virtual nets;
8 adding an access cell to said netlist; and,
9 defining said access cell as being coupled between said two
10 virtual nets.

1 17. The method of claim 16 wherein said step of modifying
2 said netlist comprises the steps of identifying a logic cell that is coupled to said
3 net, and modifying data associated with said logic cell.

1 18. The method of claim 17 wherein said data associated with
2 said logic cell comprises a name of said net, and wherein said step of modifying
3 said data associated with said logic cell further comprises changing said name.

1 19. The method of claim 16 wherein said step of modifying a
2 standard definition of said access cell stored in a cell library comprises the step
3 of modifying said definition to indicate that said access cell has two terminals.

1 20. The method of claim 16 further comprising the step of
2 creating a layout of said integrated circuit using a place and route tool, said
3 place and route tool being adapted to use said netlist and said cell library to
4 create said layout, wherein said place and route tool causes said access cell to
5 be inserted into said layout such that said net is routed through said access cell.

1 21. The method of claim 20 further comprising the steps of:
2 modifying said netlist after said layout has been created so that
3 said virtual nets are represented in said netlist as said net; and,
4 modifying said layout so that said virtual nets are represented in
5 said layout as said net.

1 22. The method of claim 16 wherein said steps of identifying a
2 net, causing said net to be represented as two virtual nets, adding an access cell
3 and defining said access cell as being coupled between said two virtual nets is
4 performed using an automated tool.

1 23. A method for enabling the automatic insertion of access
2 cells into an integrated circuit design, said method comprising the steps of:
3 modifying a standard definition of said access cells stored in a
4 cell library to specify that said access cells have two terminals; and,
5 modifying a netlist to include said access cells.

1 24. The method of claim 23 wherein said step of modifying
2 said netlist comprises the steps of:
3 identifying a set of nets in said netlist to which said access cells
4 shall be coupled;
5 identifying a set of cells in said netlist, each cell being coupled to
6 at least one of said nets;
7 modifying data associated with at least some of said cells to
8 indicate that at least some said cells are coupled to one of a set of virtual nets
9 instead of one of said nets; and,
10 adding a set of access cells to the netlist, wherein said access cells
11 are identified as being coupled between one of said nets and one of said virtual
12 nets.

1 25. The method of claim 23 further comprising the step of
2 creating a layout of said integrated circuit using a place and route tool, said
3 place and route tool being adapted to use said modified netlist and said
4 modified cell library to create said layout, wherein said place and route tool
5 causes said access cells to be inserted into said layout such that said net is
6 routed through said access cell.

1 26. The method of claim 25 further comprising the steps of:
2 modifying said modified netlist after said layout has been created
3 so that said virtual nets are represented in said netlist as said nets; and,
4 modifying said layout so that said virtual nets are represented in
5 said layout as said nets.

1 27. A computer system comprising:
2 a processor adapted to modify a netlist to cause a set of nets listed
3 in said netlist to be represented as two unique nets, and being further adapted to
4 modify said netlist to include a set of access cells, wherein said access cells are
5 defined as being coupled between different ones of said two unique nets; and,
6 a programmable medium coupled to said processor for storing
7 said netlist before and after it has been modified.

1 28. The computer system of claim 27 wherein said
2 programmable medium further stores a place and route tool executable by said
3 processor to create a layout.

1 29. The computer system of claim 27 wherein said
2 programmable medium further stores a standard cell library.

1 30. A computer program product comprising a computer
2 usable medium having computer readable program code embodied in said
3 medium that, when executed, causes a computer to:
4 receive a list that identifies a set of nets to which a set of access
5 cells shall be coupled, wherein each of said nets appearing on said list is
6 represented in said netlist as a single net;
7 modify a netlist so that each of said nets stored in said list is
8 represented in said netlist as a pair of unique nets; and,
9 modify said netlist to include a set of access cells, wherein each
10 of said access cells is defined as being connected between one of said pairs of
11 nets.

1 31. The computer program product of claim 30 wherein said
2 nets identified in said list have been entered by a user.
3

1 32. The computer program product of claim 30 wherein said
2 nets identified in said list have been generated by an algorithm that causes nets
3 to be randomly selected from said netlist.

1 33. The computer program product of claim 30 wherein said
2 computer readable program code, when executed, further causes said computer
3 to:
4 modify said netlist so that said pairs of unique nets are
5 represented in said netlist as said single nets; and,
6 modify said layout so that said pairs of unique nets are
7 represented in said layout as said single nets.

1 34. A computer program product comprising a computer
2 usable medium having computer readable program code embodied in the
3 medium that, when executed, causes a computer to:
4 identify a set of nets to which a set of access cells shall be
5 coupled, wherein each of said nets appearing on said list is represented in a
6 netlist as a single net;
7 modify said netlist so that each of said nets stored in said list is
8 represented in said netlist as a pair of unique nets; and,
9 modify said netlist to include a set of access cells, wherein each
10 of said access cells is defined as being connected between one of said pairs of
11 unique nets.

1 35. The computer program product of claim 34 wherein said
2 computer readable program code, when executed, further causes said computer
3 to:

4 determine whether each net listed in said netlist has been included
5 in a first list of nets, wherein said first list comprises nets to which access cells
6 shall be coupled;

7 add said net to said set of identified nets if said net is included in
8 said first list;

9 determine whether said net has been included in a second list of
10 nets if said net is not included in said first list, wherein said second list
11 comprises nets to which said access cells shall not be coupled;

12 not add said net to said set of identified nets if said net is included
13 in said second list;

14 determine whether said net is subject to any of a set of constraints
15 if said net has not been included in said second list of nets;

16 not add said net to said set of identified nets if said net is subject
17 to any of said constraints;

18 determine whether said net should be added to said set of
19 identified nets using an algorithm if said net is not subject to any of said
20 constraints; and,

21 add said net to said set of identified nets if, according to said
22 algorithm, said net should be added to said identified nets.

1 36. The computer program product of claim 34 wherein said
2 computer readable program code, when executed, further causes said computer
3 to:

4 execute an algorithm that causes said nets to be identified in a
5 random fashion until a predetermined percentage of all nets listed in said netlist
6 have been added to said set of identified nets.

1 37. The computer program product of claim 34 wherein said
2 computer readable program code, when executed, further causes said computer
3 to:

4 access a user-generated file; and,
5 identify said set of nets by comparing said user-generated file to
6 each of said nets in said netlist.

1 38. The computer program product of claim 37 wherein said
2 nets included in said user-generated file are associated with a portion of the
3 integrated circuit logic that is at risk for design defects.

1 39. The computer program product of claim 34 wherein said
2 computer readable program code, when executed, further causes said computer
3 to:
4 identify said set of nets by comparing each of said nets in said
5 netlist to a set of constraints.

1 40. The computer program product of claim 39 wherein one of
2 said constraints is that said net is coupled to a driving cell.

1 41. The computer program product of claim 39 wherein one of
2 said constraints is that said net is a clock net.

1 42. The computer program product of claim 39 wherein one of
2 said constraints is that said net is a test net.